

FIG. 1

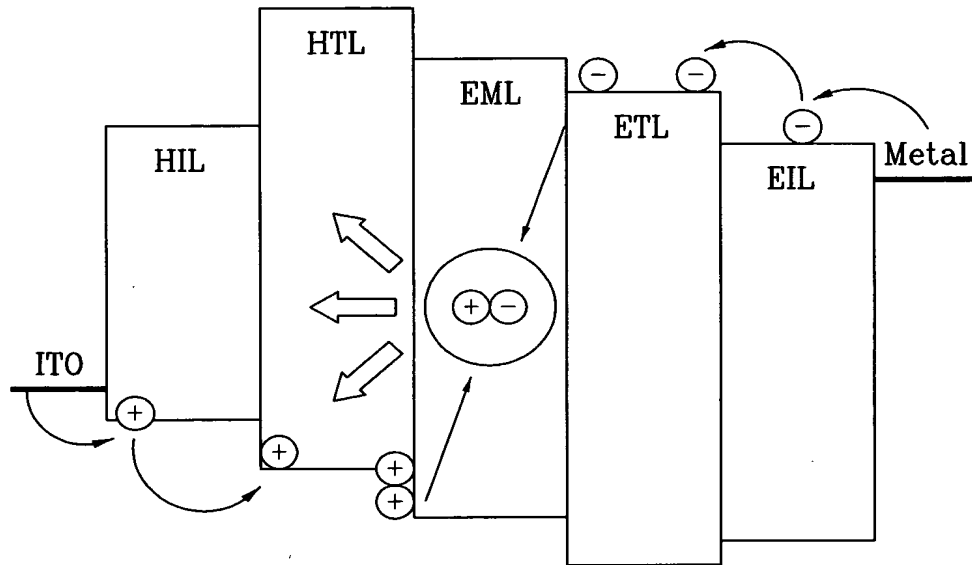


FIG. 2

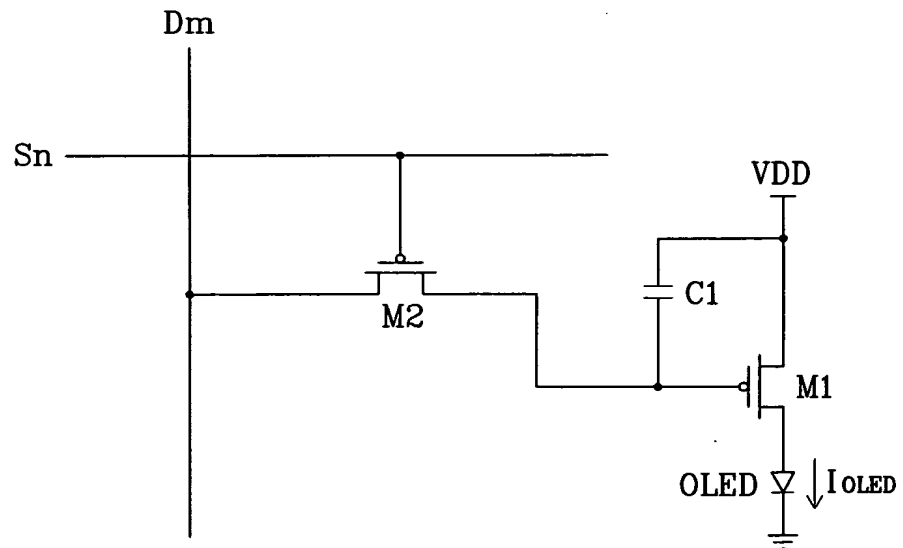


FIG. 3

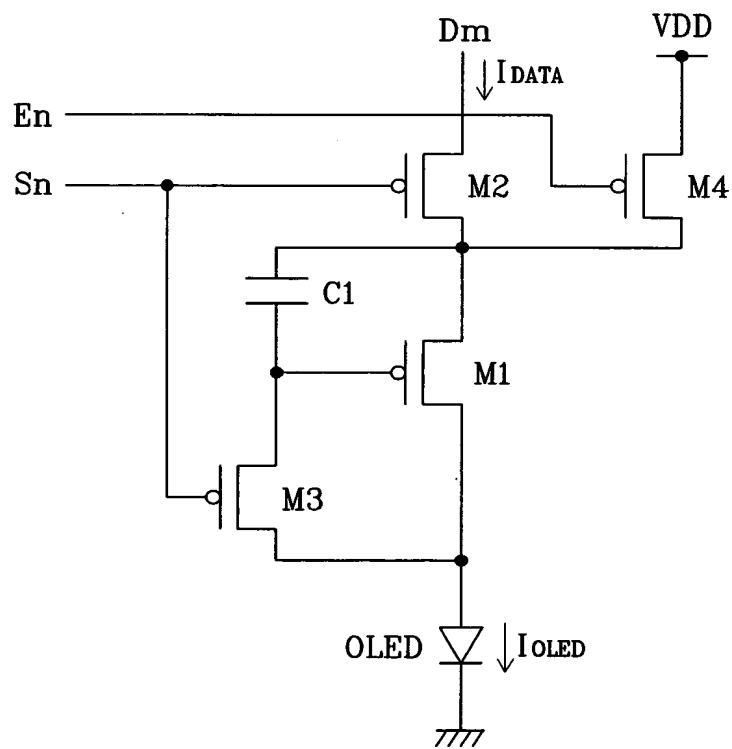


FIG. 4

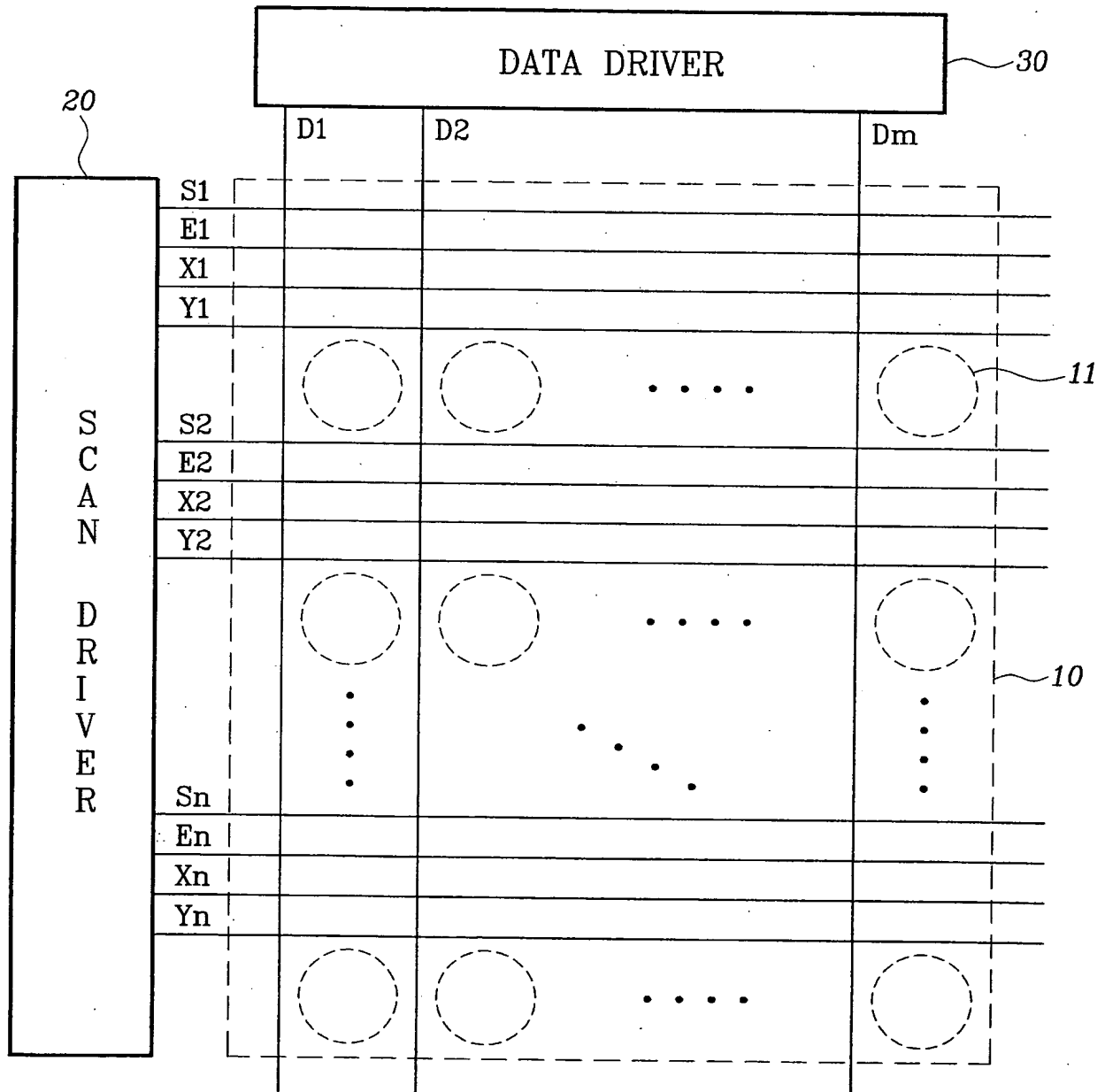


FIG. 5

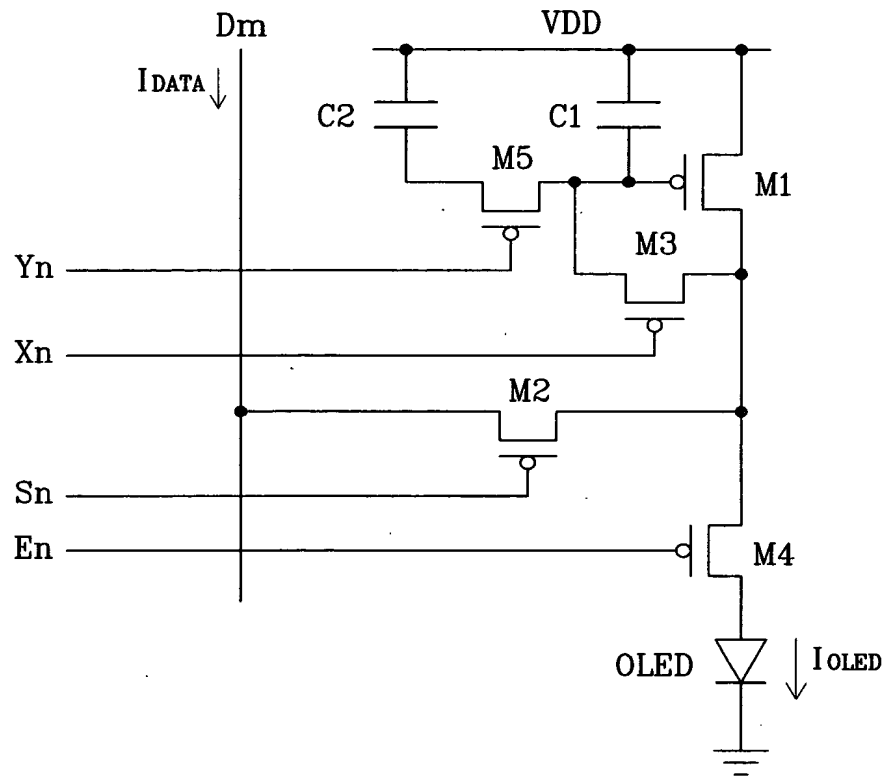
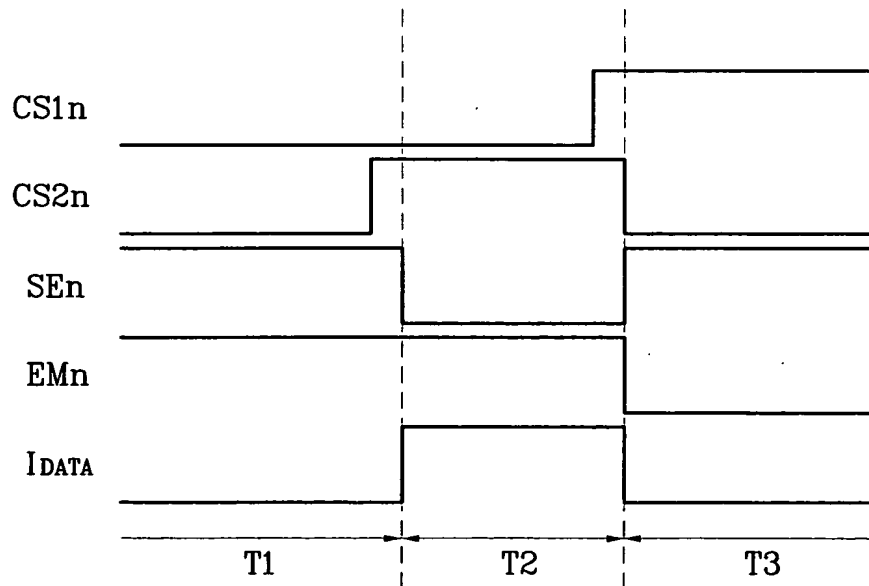


FIG. 6



Timing diagram for the 74VHC163 4-bit counter. The diagram shows five signals: CS1n, CS2n, SEn, EMn, and I_DATA over three time intervals: T1, T2, and T3. CS1n is high in T1 and T2, and low in T3. CS2n is low in T1 and T2, and high in T3. SEn is low in T1 and T2, and high in T3. EMn is high in T1 and T2, and low in T3. I_DATA is high in T1 and T2, and low in T3.

FIG. 9

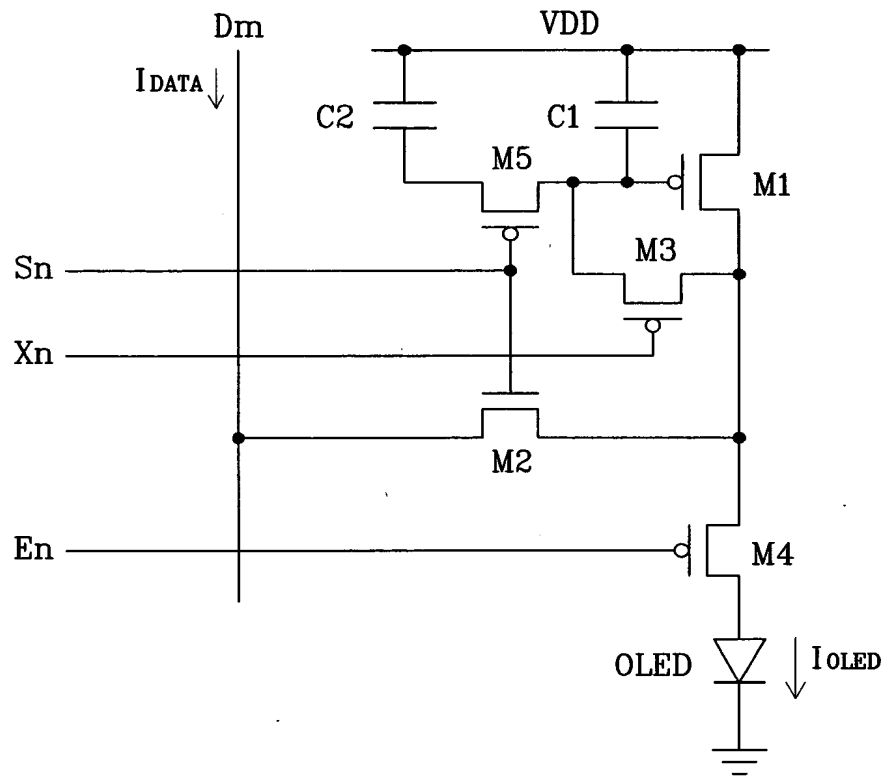
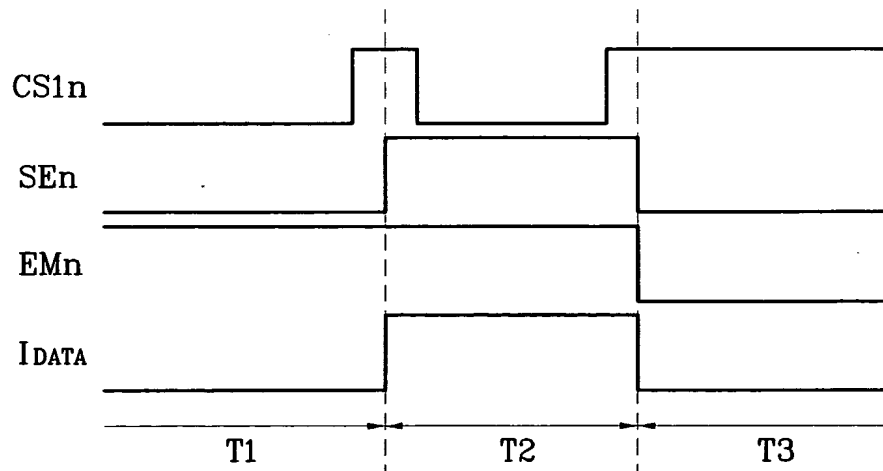


FIG. 10



[illegible]

The timing diagram shows the behavior of four signals: CS1n, SEn, EMn, and IDATA. The diagram is divided into three time periods: T1, T2, and T3, separated by vertical dashed lines.

- CS1n:** High in T1, transitions to Low at the start of T2, transitions back to High at the start of T3, and remains High.
- SEn:** High in T1, transitions to Low at the start of T2, transitions back to High at the start of T3, and remains High.
- EMn:** High in T1, transitions to Low at the start of T2, transitions back to High at the start of T3, and remains High.
- IDATA:** High in T1, transitions to Low at the start of T2, transitions back to High at the start of T3, and remains High.

FIG. 13

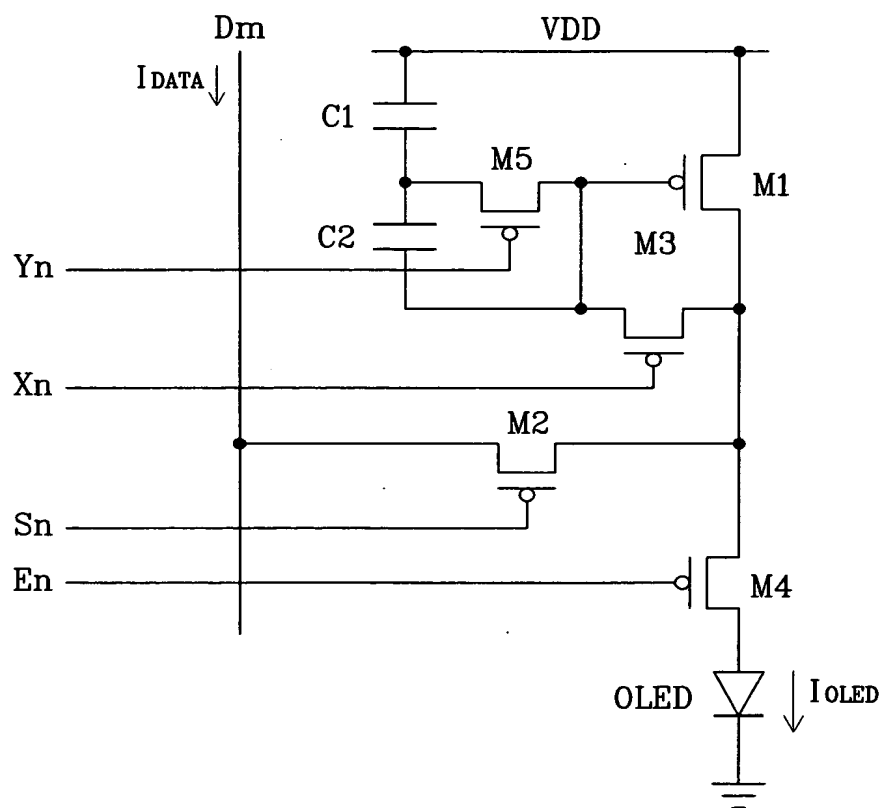


FIG. 14

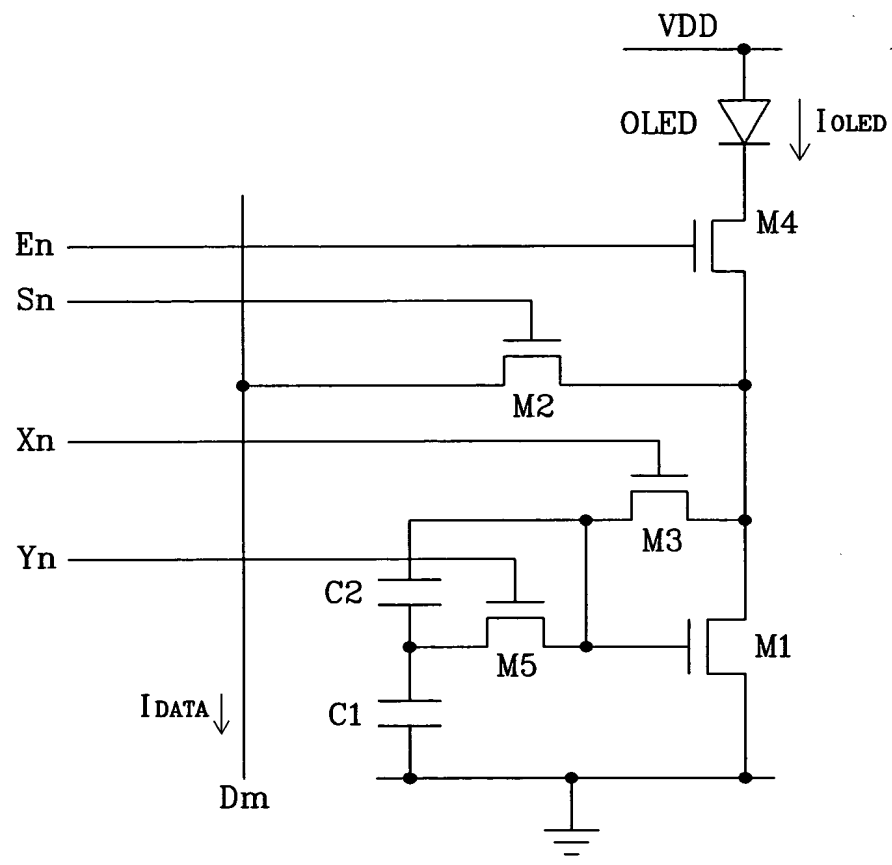


FIG.15

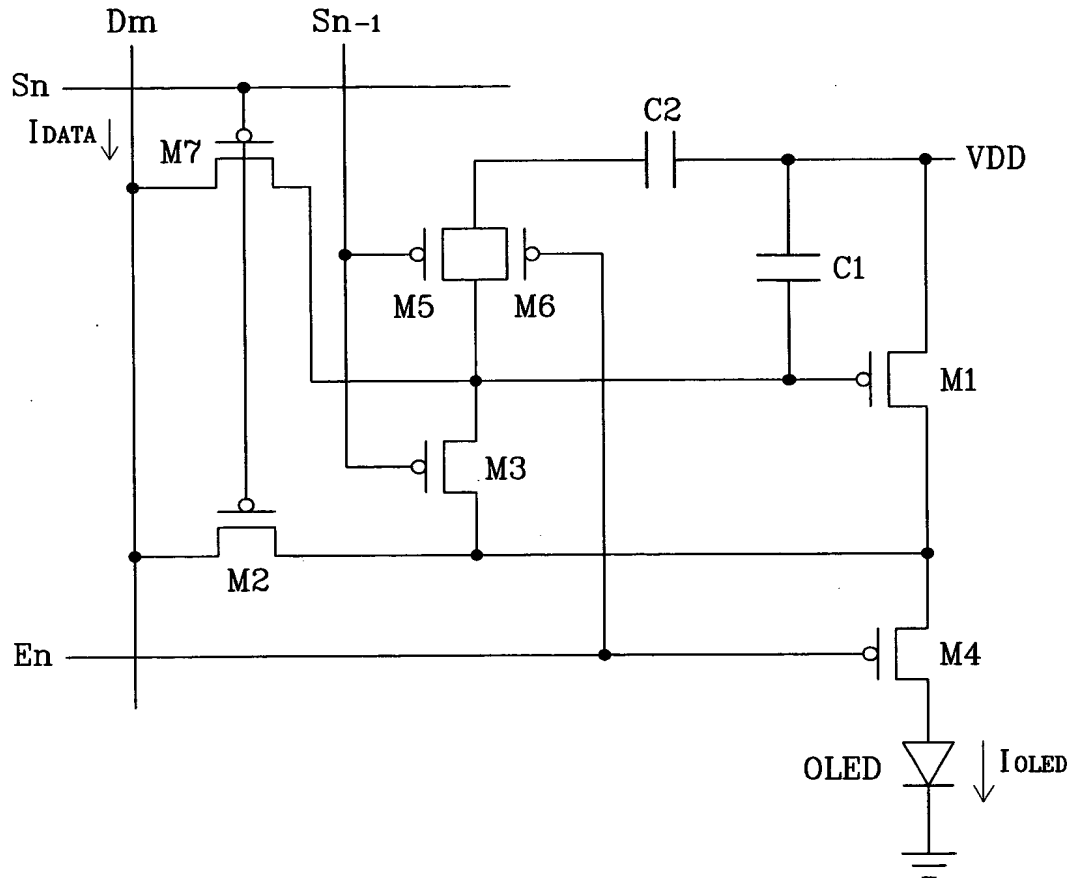


FIG.16

